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09/598,169	06/21/2000	Kenji Toyosawa	1035-270	6952

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/598,169	TOYOSAWA ET AL.	
	Examiner	Art Unit	
	Hung K. Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-16,22,25-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 28-34 are objected to because of the following informalities:

In claims 28-34, line 1, "A" should be changed to "The" for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 15, 22, 25, 26 and 29-34 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification does not disclose the level difference compensating film is disposed substantially no higher than a highest portion of the metal wiring layer, as recited in claims 15, 22 and 25. Note that Figure 6 shows the level difference compensating film (10b) is disposed higher than a highest portion of the metal wiring layer (9a,9b). Also, the specification does not disclose the level difference compensating film is in a plane common to the metal wiring layer, as recited in claims 32-34. Note that Figure 6 shows the level difference compensating film (10b) is coplanar with the upper surface of layer (10a).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 14, 15, 22 and 25-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Narui et al. (PN 6,150,689, of record).

Narui et al. discloses, as shown in Figures 54, 55 and 61, a semiconductor device, comprising:

an active element provided on a semiconductor substrate, the active element including at least two diffusion layers (15) and a gate electrode (8C);

a metal wiring layer (30A,30B) provided on the active element;

an interlayer insulating film (27,31,32) covering the active element;

a pad metal (41B) for an electrode pad forming an external electrical terminal for the semiconductor device, the pad metal being provided over the interlayer insulating film and substantially covering the at least two diffusion layers and the gate electrode of the active element, wherein the active element is on a side of the interlayer insulating film opposite to the pad metal;

a barrier metal layer provided over the active element and the interlayer insulating film, so that the pad metal is provided on the barrier metal layer and covering the active element, wherein:

the interlayer insulating film has at least a level difference compensating film for compensating for a level difference of the metal wiring layer;

a portion of the level difference compensating film under the pad metal is removed.

With regard to claim 15, Narui et al. discloses, as shown in Figures 54, 55 and 61, a semiconductor device comprising:

an active element provided on a semiconductor substrate, the active element including at least two diffusion layers (15) and a gate electrode (8C);

a metal wiring layer (30A,30B) provided on the active element;

an interlayer insulating film (27,31,32) covering the active element;

a pad metal (41B) for an electrode pad forming an external electrical terminal for the semiconductor device, the pad metal being provided over the interlayer insulating film and substantially covering the at least two diffusion layers and the gate electrode of the active element, wherein the active element is on a side of the interlayer insulating film opposite to the pad metal;

a barrier metal layer provided on the active element and the interlayer insulating film, so that the pad metal is provided on the barrier metal layer and covering the active element, wherein:

the interlayer insulating film has at least a level difference compensating film for compensating for a level difference of the metal wiring layer;

the level difference compensating film is formed to a minimum thickness necessary for compensating for the level difference of the metal wiring layer.

With regard to claim 22, Narui et al. discloses, as shown in Figures 54, 55 and 61, a semiconductor device comprising:

an active element provided on a semiconductor substrate, the active element including at least two diffusion layers (15) and a gate electrode (8C);

a lower interlayer insulating film (17,18,19) formed to cover the active element;

a metal wiring layer (30A,30B) provided on the lower interlayer insulating film;

an upper interlayer insulating film (27,31,32) formed to cover the metal wiring layer;

a pad metal (41B) for an electrode pad forming an external electrical terminal for the semiconductor device, the pad metal being provided over the upper interlayer insulating film and substantially covering the at least two diffusion layers and the gate electrode of the active element, wherein the active element is on a side of the upper and lower interlayer insulating films opposite to the pad metal;

another metal wiring layer (35B) formed over the active element;

wherein each of the lower and upper interlayer insulating films have a trilaminar structure, each of a first layer and a third layer of the trilaminar film being silicon nitride film, while a second layer of the trilaminar film being formed of glass;

the second layer of the upper interlayer insulating film formed to a minimum thickness necessary for compensating the level difference of the metal wiring layer.

With regard to claim 25, Narui et al. discloses, as shown in Figures 54, 55 and 61, a semiconductor device comprising:

an active element provided on a semiconductor substrate, the active element including at least two diffusion layers (15) and a gate electrode (8C);

a first metal wiring layer (30A,30B) formed over the active element;

a plurality of other metal wiring layer (BL1,BL2,35,35B) above the active element;

a plurality of interlayer insulting films (29,31,32,38,39,40) each being provided between a pair of the metal wiring layers wherein the plurality of interlayer insulating films and plurality of metal wiring layers are vertically aligned above the active element;

wherein each interlayer insulating film has a multilayer structure including at least a glass film sandwiched between insulating films formed of a silicon nitride film;

further wherein the film formed of glass in the interlayer insulating film is formed to a minimum thickness necessary for compensating for a level difference of one of the metal wiring layers;

a pad metal (YS,41B) for an electrode pad forming an external electrical terminal for the semiconductor device, the pad metal being provided over the interlayer insulating films.

With regard to claim 26, Narui et al. discloses the pad metal substantially covers at least two diffusion layers and the gate electrode of the active element, and the active element is on a side of the interlayer insulting film opposite to the pad metal.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narui et al. (PN 6,150,689, of record) in view of Hosomi et al. (PN 5,773,888, of record).

With regard to claim 16, Narui et al. taught the invention substantially as claimed, including the semiconductor device as recited in the rejection of claim 14. Narui et al. does not teach a passivation film being covering a large part of the pad metal and an aperture in the passivation film having an edge adjacent an inside edge of the pad metal. However, Hosomi et al. taught a semiconductor device comprising a passivation film (3) being covering a large part of the pad metal (2) and an aperture (9) in the passivation film having an edge adjacent an inside edge of the pad metal [Figure 1 and Col. 4, lines 42-67]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Narui et al. having a passivation film being covering a large part of the pad metal and an aperture in the passivation film having an edge adjacent an inside edge of the pad metal, such as taught by Hosomi et al. in order to protect the device from external contamination.

With regard to claim 16, Narui et al. and Hosomi et al. taught the device further comprising another barrier metal layer (4) providing on the passivation film and the pad metal which is exposed by a window in the passivation film [Figure 1 and Col. 5, lines 1-15].

5. Claims 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narui et al. (PN 6,150,689, of record) in view of Ng (PN 5,843,839, of record).

Narui et al. taught the invention substantially as claimed, including the semiconductor device as recited in the rejection above. Narui et al. further teaches the pad metal is connected to the metal wiring layer via a through-hole in the interlayer insulating film. Narui et al. does not teach the through-hole not penetrate the level difference compensating film. However, Ng discloses the interlayer insulating layer having a level difference compensating film or the film of spin-on-glass (16) being coplanar with the first layer (15). Note Figures 8 and 12 of Ng. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the interlayer insulating film of Narui et al. having the level difference compensating film or the film of spin-on-glass being coplanar with the first layer, such as taught by Ng so that the through-hole not penetrate the level difference compensating film in order to reduce the overall thickness of the interlayer insulating layer and to increase the circuit density of the device.

Response to Arguments

6. Applicant's arguments filed 11/19/03, 12/01/03 and 12/05/03, have been fully considered but they are not persuasive.

It is argued, at pages 9-11 of the Remarks, filed 11/19/03, that wiring layer 41B is an interconnect layer and not a pad metal for an electrode pad nor an external electrical terminal. This argument is not convincing because wiring layer 41B is capable to function as a pad metal for an electrode pad or an external electrical terminal.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., only a portion of a level

difference compensating layer of an interlayer insulating film covering an active element and the level difference compensating film is not formed on the uppermost metal wiring layer but only formed between the metal wiring layers) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It is argued, at page 12 of the Remarks, that Narui et al. do not disclose a lower interlayer insulating film formed so as to cover the active element because layers 17, 18 and 19 of Narui et al. do not cover the diffusion layers 15 of the active element. This argument is not convincing because layers 17, 18 and 19 of Narui et al. does cover the diffusion layers 15 of the active element. Note that claim language does not specifically state whether the lower inlayer insulating film completely cover the diffusion layers, therefore, Applicants' claim 22 does not distinguish over the Narui et al. reference.

It is argued, at page 12 of the Remarks, that Narui et al. do not disclose a plurality of multilayer interlayer insulating film. This argument is not convincing because Narui et al. discloses, as shown in Figures 54, 55 and 61, a plurality of interlayer insulting films (29,31,32,38,39,40). Therefore Applicants' claim 25 does not distinguish over the Narui et al. reference.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching,

suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would be motivated to form a passivation film covering a large part of the pad metal and an aperture in the passivation film having an edge adjacent an inside edge of the pad metal in order to protect the device from external contamination.

It is argued, at page 9 of the Remarks, filed 12/01/03, that Narui et al. does not disclose placing a level compensating film on the same level as a wiring layer. This argument is not convincing due to the above rejection of 35 USC 112, first paragraph, as new matter situations.

It is argued, at page 10 of the Remarks, filed 12/05/03, that Narui et al. does not discloses removing a portion of the SOG film. This argument is not convincing because the Naguie et al. teaches removing a portion of the SOG film to form the contact through-hole.

It is argued, at page 9 of the Remarks, filed 12/05/03, that Narui et al. does not discloses placing a level compensating film that is substantially no higher than metal wiring layers. This argument is not convincing due to the above rejection of 35 USC 112, first paragraph, as new matter situations. Also the features upon which applicant relies (i.e., substantially only between metal wiring layers) are not recited in the rejected claim(s).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

March 09, 2004

Hung Vu

Patent Examiner